AMENDMENTS

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Previously Presented) A method for scheduling access to a device comprising:

tracking a current state of a device;

tracking a count of a number of scheduled requests which require the current state;

storing a configurable switch point, wherein the configurable switch point includes a threshold value to indicate when to switch from the current state to an alternate state of the device; and

switching the state of the device after:

determining the count reaches the threshold value established for the switch point; and

receiving one or more incoming requests which require the alternate state of the device.

2. (Original) The method as set forth in claim 1, further comprising configuring the switch point.

3. (Previously Presented) The method as set forth in claim 2, wherein the switch point is dynamically configurable by software.

4. (Canceled)

5. (Previously Presented) The method as set forth in claim 1, wherein the device is a dynamic random access memory (DRAM), the method further comprising selecting a scheduler type from the group consisting of a DRAM bus turnaround scheduler, a DRAM page scheduler, and a DRAM physical bank switching scheduler.

6. (Previously Presented) A bus scheduler comprising:

an input configured to receive at least one incoming request, each request indicating a bus direction;

a register to store a configurable switch point, wherein the configurable switch point includes a threshold value to indicate when to switch from the current state to an alternate state of the device;

an indicator of a current bus direction;

a unit to track a count of requests processed using the current bus direction; and

logic configured to switch the direction of the bus to process incoming requests after the count reaches the threshold value established for the switch point and there are incoming requests having the direction opposite to the current direction of the device bus.

7. (Previously Presented) The bus scheduler as set forth in claim 6, wherein the threshold value established for the switch point is dynamically configurable.

8. (Previously Presented) A scheduler comprising:

a first unit to track a current state of a device;

a second unit to track a count of requests that require a particular state;

a register to store a configurable switch point, wherein the configurable switch point includes a threshold value to indicate when to switch from the current state to an updated device state;

logic configured to facilitate the updated device state when the count crosses the threshold of the switch point; and

scheduling logic configured to schedule access requests to the device using the updated device state.

9. (Previously Presented) The scheduler as set forth in claim 8, wherein a value of the threshold established for the switch point is dynamically configurable via software.

10. (Original) The scheduler as set forth in claim 8 wherein the device comprises a bus and the device state comprises a bus direction, said scheduling dependent upon the bus direction.

11. (Original) The scheduler as set forth in claim 8, wherein the device is a dynamic random access memory (DRAM) and scheduling is selected from the group consisting of DRAM bus turnaround scheduling, DRAM page scheduling and DRAM physical bank switching.

12. (Canceled)

13. (Original) The scheduler as set forth in claim 8, wherein the device comprises a DRAM with multiple pages and the device state comprises the identity of at least one open page, said scheduling dependent on the at least one page opened.

14. (Original) The scheduler as set forth in claim 8, wherein the device comprises a DRAM with multiple physical banks and the device state comprises the last accessed physical bank, said scheduling dependent on the last accessed physical bank.

15. (Canceled)

16. (Canceled)

17. (Previously Presented) The scheduler as set forth in claim 8, wherein the scheduler is embedded on a System on a Chip.

18. (Previously Presented) The bus scheduler as set forth in claim 6, wherein the bus scheduler is embedded on a System on a Chip.

19. (Previously Presented) The scheduler as set forth in claim 8, further comprising:

a controller of a volatile memory coupled to the scheduler; and

filter logic configured to combine thread quality of service scheduling and volatile memory scheduling to reorder servicing requests from one or more threads based on achieving a highest usage efficiency of the volatile memory while still satisfying quality of service guarantees for each thread.

20. (Previously Presented) The bus scheduler as set forth in claim 6, further comprising:

a controller of a volatile memory coupled to the scheduler via the bus; and

filter logic configured to combine thread quality of service scheduling and volatile memory scheduling to reorder servicing requests from one or more threads based on achieving a highest usage efficiency of the volatile memory while still satisfying quality of service guarantees for each thread.

21. (Previously Presented) An apparatus to scheduling access to a device comprising:

means for tracking a current state of a device;

means for tracking a count of a number of scheduled requests which require the current state;

means for storing a configurable switch point, wherein the configurable switch point includes a threshold value to indicate when to switch from the current state to an alternate state of the device; and

means for switching the state of the device after:

determining the count reaches the threshold value established for the switch point; and

receiving one or more incoming requests which require the alternate state of the device.

22. (Previously Presented) The apparatus of claim 19, wherein the logic is further configured to empirically determine the switch point based upon past performance of the filter logic.

23. (Previously Presented) The apparatus of claim 22, wherein the logic is further configured to implement a count and compare function to determine the switch point.

24. (Previously Presented) The apparatus of claim 8, further comprising reset logic to reset the count.

25. (Previously Presented) The apparatus of claim 24, wherein the second unit is further configured to restart the count in response to a count reset and one or more incoming requests which require the updated device state.

26. (Previously Presented) The apparatus of claim 20, wherein the logic is further configured to empirically determine the switch point based upon past performance of the filter logic.

27. (Previously Presented) The apparatus of claim 26, wherein the logic is further configured to implement a count and compare function to determine the switch point.

28. (Previously Presented) The apparatus of claim 6, further comprising reset logic to reset the count.

29. (Previously Presented) The apparatus of claim 28, wherein the unit is further configured to restart the count in response to a count reset and a determination that there are the incoming requests having a direction opposite to the current direction of the device bus.